REMARKS

Summary of the Amendment

Upon entry of the present amendment, Claim 20 will have been amended. Accordingly, Claims 1-20 remain currently pending. For the reasons set forth below, Applicant submits that each of the pending claims is allowable over the art, and an indication of allowability of the present application is respectfully requested.

Summary of the Office Action

In the subject Office Action, Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over the art of record.

Traversal of Rejection Under 35 U.S.C. §103(a)

OTSUKA in View of HIYOSHI

Applicant respectfully traverses the rejection of Claims 1-6 and 8-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,402,318 to Otsuka et al. [hereinafter "OTSUKA"] and U.S. Patent Application Publication No. 2002/0038873 to Hiyoshi [hereinafter "HIYOSHI"].

A Review of OTSUKA

As shown in FIGS. 6 through 12, a semiconductor device 101 is provided having a semiconductor chip 102 which is disposed in a region (or void) defined by a surrounding inner peripheral edge of an interposer 103. The chip 102 and interposer 103 are mounted on the central portion of support plate 104 through an adhesive layer. The segments of the inner peripheral edge of the interposer 103 face and extend along respective sides of the semiconductor chip 102. The interposer 103 has a pair of recessed shoulders formed in its upper surface about the inner and outer peripheral edges of thereof. The outer recessed shoulder of the interposer 103 is connected to leads 105 extending radially in four directions. As shown in FIGS. 9 through 12, the interposer 103 includes a flat, sheet-like ground wire 107 which is bonded to the support plate 104 with an insulating adhesive 106. Signal lines

109 are positioned over the ground line 107 through an insulating film 108 made of a glass fiber-reinforced resin or a polyimide tape. A flat, sheet-like power source line 110 is positioned over signal lines 109 through another sheet of insulating film 108, and a protective film 115 is deposed on the power source line 110.

A Review of HIYOSHI

Figure 8 of HIYOSHI discloses an Insulated Gate Bi-polar Transistor (IGBT) module. The IGBT module 30 comprises base plate 31, copper plate 38 attached by solder 39 to the top of base plate 31, insulative ceramic substrate 32 affixed to the top of copper plate 38, emitter/gate wiring elements 43-1 through 43-3, IGBT chip 33, intermediate wiring element 51, emitter terminal 35-1, collector terminal 35-2, gate terminal 35-3, resin case 36 and resin cap 37. The intermediate wiring elements 51 are provided only at locations that require insulation and are attached over the outer perimeter of chip 33 via insulative bonding resin 41.

Examiner's Rejection of Independent Claim 1

Regarding Claim 1, the Examiner submits that OTSUKA (Figures 8-12) teaches an interposer for use in a semiconductor package, the interposer comprising: an interposer body 103 molded from a dielectric material, the interposer body 103 defining opposed top (an upper surface of 103) and bottom (a bottom surface of 103) surfaces, an outer peripheral edge (a portion of outer edge of 103), and an inner peripheral edge (a portion of the inner edge of 103); a die pad (a portion of die pad 104, which is formed under the chip 102) having opposed top (an upper surface of the die pad 104) and bottom (a bottom surface of the die pad 104) surfaces and a peripheral edge (a portion of peripheral edge of the die pad 104), the inner peripheral edge of the interposer body 103 and the top surface of the die pad 104 collectively defining a cavity of the interposer; the die pad 104 being embedded within the interposer body such that the bottom surface of the die pad (a portion of the die pad, which is formed under the chip 102) is exposed in and substantially flush with the bottom surface of the interposer body 103.

However, the Examiner admits that OTSUKA differs from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top

surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land; and the interposer body forming a non-conductive barrier between each of the interposer leads and between the interposer leads and the die pad. The Examiner then argues that HIYOSHI (Figure 8) shows a plurality of electrically conductive elements (wiring 51) formed on the top surface of the die pad (the die pad is formed under the chip 33), and defining a land, and the non-conductive barrier layer (insulation resin 41) formed between the conductive layer 51 and the die pad. Then the Examiner concludes, that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package.

Applicant's Independent Claim 1

Applicant's independent Claim 1 recites, *inter alia*, an interposer body molded from a dielectric material, the interposer body defining opposed top and *bottom surfaces*, an outer peripheral edge, and an inner peripheral edge; . . . , the die pad being embedded within the interposer body *such that the bottom surface of the die pad is exposed in and substantially flush with the bottom surface of the interposer body*, ...

The invention recited in Independent Claim 1 does not result from the proposed modification and/or combination of OTSUKA in view HIYOSHI

Neither OTSUKA or HIYOSHI, whether considered individually or in combination, teach the aforementioned features recited in independent Claim 1. For instance, the OTSUKA support plate 104 ***is not embedded within the interposer body 103***. Instead, the OTSUKA support plate 104 is attached to the chip 102 and interposer 103 by insulative adhesive 106 as is best illustrated in Figures 10-12. Furthermore, HIYOSHI does not teach or suggest any feature that resembles Applicant's interposer features as recited in independent Claim 1.

Applicant submits that, as neither OTSUKA and HIYOSHI teaches or suggests, *inter alia*, . . . , the die pad being embedded within the interposer body *such that the bottom surface of the die pad is exposed in and substantially flush with the bottom surface of the*

interposer body, ... no proper combination of these references can render unpatentable the combination of features recited in at least independent Claim 1.

Therefore, even if OTSUKA and HIYOSHI are properly combined (which Applicant disputes), the invention recited in Applicant's independent Claim 1 still does not result.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 1 under 35 U.S.C. §103(a) and indicate that these claims are allowable.

Additionally, there is no apparent motivation to modify and/or combine OTSUKA in view of HIYOSHI

Moreover, Applicant submits that there is no motivation to even combine OTSUKA and HIYOSHI as the Examiner has proposed.

For instance, as discussed *supra*, the Examiner admits that OTSUKA differs from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land, the interposer body forming a non-conductive barrier between each of the interposer leads and between the interposer leads and the die pad. The Examiner then argues that HIYOSHI (Figure 8) shows a plurality of electrically conductive elements (wiring 51) formed on the top surface of the die pad (the die pad is formed under the chip 33), and defining a land, and the non-conductive barrier layer (insulation resin 41) formed between the conductive layer 51 and the die pad. The Examiner then concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package.

As best understood, this proposed modification still does not satisfy what the Examiner admits is missing from the OTSUKA reference, in particular, a plurality of electrically conductive interposer leads *embedded within the top surface of the interposer body* and at least partially exposed therein, each of the interposer leads defining a land; . . . Moreover, there does not appear to be any reason or rationale whatsoever (i.e., motivation) "to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package."

Accordingly, because there appears to no requisite motivation to combine OTSUKA with HIYOSHI (or modify OTSUKA in view of HIYOSHI), Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 1 under 35 U.S.C. §103(a) and indicate that this claim is allowable.

Dependent Claims 2-10

Further, for the foregoing reasons, Applicant submits that dependent Claims 2-10 are allowable at least for the reason that these claims depend from allowable independent Claim 1 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of dependent Claims 2-10 under 35 U.S.C. §103(a) and indicate that these claims are allowable.

Examiner's Rejection of Independent Claim 11

Regarding Claim 11, the Examiner submits that OTSUKA (Figures 8-12) teaches an interposer for use in a semiconductor package, the interposer comprising: a die pad (a portion of the die pad 103, which is formed under the chip 102) having opposed top (an upper surface of the die pad) and bottom (a bottom surface of the die pad) surfaces and a peripheral edge; a layer of adhesive tape (a portion of the adhesive layer; column 7, lines 15-18) attached to the top surface of the die pad, the layer of the top surface of the die pad collectively defining a cavity of the interposer.

However, the Examiner admits that OTSUKA differs from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land. The Examiner submits that HIYOSHI (Figure 8) shows a plurality of electrically conductive elements 51 formed on the top surface of the die pad (the die pad is formed under the chip 33), and defining a land. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package.

Applicant's Independent Claim 11

Applicant's independent Claim 11 recites, inter alia, ... *a layer of adhesive tape attached to the top surface of the die pad and extending along the peripheral edge thereof,* the layer and the top surface of the die pad collectively defining a cavity of the interposer; and a plurality of electrically conductive interposer leads attached to the adhesive tape and extending at least partially about the die pad in spaced relation to each other, each of the interposer leads defining a land.

The invention recited in Independent Claim 11 does not result from the proposed modification and/or combination of OTSUKA in view HIYOSHI

Neither OTSUKA or HIYOSHI, whether considered individually or in combination teach the aforementioned features recited in independent Claim 11. For instance, OTSUKA does not teach, inter alia, ... *a layer of adhesive tape attached to the top surface of the die pad and extending along the peripheral edge thereof,* the layer and the top surface of the die pad collectively defining a cavity of the interposer; . . . .

Applicant submits that, as neither OTSUKA and HIYOSHI teaches or suggests, inter alia, ... *a layer of adhesive tape attached to the top surface of the die pad and extending along the peripheral edge thereof,* the layer and the top surface of the die pad collectively defining a cavity of the interposer; . . . no proper combination of these references can render unpatentable the combination of features recited in at least independent Claim 11.

Therefore, even if OTSUKA and HIYOSHI are properly combined (which Applicant disputes), the invention recited in Applicant's independent Claim 11 still does not result.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 11 under 35 U.S.C. §103(a) and indicate that this claim is allowable.

Also, as previously asserted, there is no apparent motivation to modify and/or combine OTSUKA and HIYOSHI

As discussed *supra*, Applicant submits that there is no motivation to even combine OTSUKA and HIYOSHI in the manner proposed by the Examiner.

As best understood, the proposed modification still does not satisfy what the Examiner admits is missing from the OTSUKA reference, in particular, a plurality of electrically conductive interposer leads *embedded within the top surface of the interposer body* and at least partially exposed therein, each of the interposer leads defining a land; . . . . . Moreover, there does not appear to be any reason or rationale (i.e., motivation) "to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package."

Accordingly, because there appears to be no requisite motivation to combine OTSUKA with HIYOSHI (or modify OTSUKA in view of HIYOSHI), Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 11 under 35 U.S.C. §103(a) and indicate that this claim is allowable.

Dependent Claims 12-19

Further, for the foregoing reasons, Applicant submits that dependent Claims 12-19 are allowable at least for the reason that these claims depend from allowable independent Claim 11 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of dependent Claims 12-19 under 35 U.S.C. §103(a) and indicate that these claims are allowable.

Examiner's Rejection of Independent Claim 20

With regard to Claim 20, the Examiner argues that OTSUKA (Figures 8-12) teaches an interposer for use in a semiconductor package, the interposer comprising: a die pad (a portion of the die pad, which is formed under the chip 102) having opposed top (an upper surface of the die pad 104) a bottom (a bottom surface of the die pad 104) surfaces and a peripheral edge.

However, the Examiner admits that OTSUKA differs from the claimed invention by not showing a plurality of electrically conductive interposer leads embedded within the top surface of the interposer body and at least partially exposed therein, each of the interposer leads defining a land; and the interposer body forming a non-conductive barrier between each

of the interposer leads and the die pad. Then, the Examiner argues that HIYOSHI (Figure 8) shows a plurality of electrically conductive elements (wiring 51) formed on the top surface of the die pad (the die pad is formed under the chip 33) and defining a land, and the non-conductive barrier layer (insulation resin 14) formed between the conductive layer 51 and the die pad. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of HIYOSHI into the device taught by OTSUKA because the leads provide interconnections in the semiconductor package.

Applicant's Independent Claim 20

Applicant's independent Claim 20 recites, *inter alia*, ... *a land which projects downwardly from the finger portion and has a bottom terminal surface which is generally coplanar with the bottom surface of the die pad*; . . . .

The invention recited in Independent Claim 20 does not result from the proposed modification and/or combination of OTSUKA in view HIYOSHI

Neither OTSUKA or HIYOSHI, whether considered individually or in combination teach the aforementioned features recited in independent Claim 20. For instance, OTSUKA does not teach, *inter alia*, ... a land which projects downwardly from the finger portion and has a bottom terminal surface which is generally coplanar with the bottom surface of the die pad; . . . . Furthermore, HIYOSHI similarly does not teach at least the aforementioned features.

Applicant submits that, as neither OTSUKA and HIYOSHI teaches or suggests the aforementioned features of amended Claim 20, no proper combination of these references can render unpatentable the combination of features recited therein.

Therefore, even if OTSUKA and HIYOSHI are properly combined (which Applicant disputes), the invention recited in Applicant's independent Claim 20 still does not result.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 20 under 35 U.S.C. §103(a) and indicate that this claim is allowable.

And, as previously asserted, there is no apparent motivation to modify and/or combine OTSUKA and HIYOSHI

As discussed *supra*, Applicant submits that there is no motivation to even combine OTSUKA and HIYOSHI in the manner proposed by the Examiner.

Accordingly, because there appears to no requisite motivation to combine OTSUKA with HIYOSHI (or modify OTSUKA in view of HIYOSHI), Applicant requests that the Examiner reconsider and withdraw the rejection of independent Claim 20 under 35 U.S.C. §103(a) and indicate that this claim is allowable.

CONCLUSION

Applicant respectfully submits that each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. §103, and respectfully requests that the Examiner indicate such allowance.

In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof, anticipate or render obvious Applicant's invention, as recited in each of Claims 1-20. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Further, any amendments to the claims which have been made in this response and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppels should be deemed to attach thereto.

Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein is respectfully requested and now believed to appropriate.

Should there be any questions or comments, the Examiner is invited to contact the undersigned at telephone number listed below.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

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